UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,861,326 B2
APPLICATION NO. : 09/989931
DATED : March 1, 2005
INVENTOR(S) : Gonzalez et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, Item (56), "References Cited", "U.S. PATENT DOCUMENTS",
Insert --4,903,108 2/1990 Young et al.
5,650,343 7/1997 Luning et al.--
Before "5,759,908".

Title Page, Item (56), "References Cited", "U.S. PATENT DOCUMENTS",
Insert --6,306,691 B1 10/2001 Koh--
Before "6,358,806 B1".

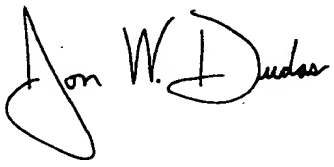
Title Page, Item (56), "References Cited", "U.S. PATENT DOCUMENTS",
Insert --6,566,210 B2 5/2003 Ajmera et al.--
Before "6,620,671 B1".

Title Page, Item (56), "References Cited", "U.S. PATENT DOCUMENTS",
Insert --6,653,714 B2 11/2003 Matsuno et al.--
Before "2001/0008292 A1".

Title Page, Item (56), "References Cited",
Insert --OTHER PUBLICATIONS
Lee, W. et al., "Investigation of Poly-$Si_{1-x}Ge_x$ for Dual-Gate CMOS Technology", IEEE Electron Device Letters, Vol. 19, No. 7, July 1998, pp. 247-249.
Wolf, S., "Silicon Processing for the VLSI Era: Vol. 1: Process Technology", 1986 Lattice Press, pp. 191-195.
Before "* cited by examiner".

Signed and Sealed this

First Day of August, 2006



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